

configured to generate a second reference current, and a second voltage adjustment module configured to increase the voltage of the gate of the switching transistor if the second intermediate current is greater than the second reference current.

[0020] According to one embodiment, the switching transistor is of the pMOS type.

[0021] According to another embodiment, the first and second voltage adjustment modules respectively comprise a transistor of the pMOS type whose source is coupled to the larger of the first and second voltages and whose drain is coupled to the gate of the switching transistor.

[0022] According to yet another embodiment, the first and second reference current modules are substantially identical, the first and second reference currents are substantially identical, and the first and second voltage adjustment modules are substantially identical.

[0023] Advantageously, the circuit can for example be embodied in an integrated manner.

[0024] According to another aspect, there is proposed an electronic system, notably powered by at least one battery, comprising at least one circuit such as defined hereinabove.

[0025] According to yet another aspect, there is proposed an electronic apparatus, such as cellular mobile telephone, tablet, or laptop computer, comprising at least one system such as defined hereinabove.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] Other advantages and characteristics of the invention will become apparent on examining the detailed description of wholly non-limiting modes of implementation and embodiments, and the appended drawings in which:

[0027] FIGS. 1 to 4 schematically illustrate modes of implementation and embodiments of the invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0028] The reference 1 in FIG. 1 designates an electronic apparatus, here, for example, a cellular mobile telephone powered by a battery BAT.

[0029] The mobile telephone 1 comprises an electronic system SE embodied in an integrated manner. The electronic system SE furthermore comprises an electronic circuit CE comprising a Low-DropOut voltage regulator 2, a charge switch circuit 3, a decoupling capacitor 4, and a charge circuit 5. The Low-DropOut voltage regulator 2 is of conventional structure and is commonly known by the person skilled in the art by the acronym "LDO." This regulator 2 is coupled between the voltage VBAT of the battery and the ground GND and provides an output voltage VOUT at an output terminal BS.

[0030] The charge switch circuit 3 is coupled between an input terminal BE and the output terminal BS of the low-dropout voltage regulator 2. The decoupling capacitor 4 is coupled between the output terminal BS and the ground GND. The charge circuit 5 in this example is a Universal Integrated Circuit Card, commonly known by the person skilled in the art by the acronym "UICC."

[0031] By way of non-limiting example, the input terminal BS can be coupled to a power supply rail provided by the electronic system SE and being different from that of the battery voltage VBAT. The input terminal BE can, for example, receive an input voltage VIN whose value is

greater than zero and less than or equal to the voltage VBAT of the battery. The voltage VIN can be provided by a power supply source, a low-voltage dropout regulator for example.

[0032] The mobile telephone 1 can operate in several modes, including a normal mode and a standby mode.

[0033] When the telephone 1 is operating in the normal mode, the voltage regulator 2 is powered by the voltage VBAT and delivers the output voltage VOUT at the output terminal BS. The charge switch circuit 3 is in the "off" state and consequently the charge circuit 5 and the decoupling capacitor 4 are powered by the output voltage VOUT.

[0034] When the telephone 1 is operating in the standby mode, the voltage regulator 2 is disconnected and the charge switch circuit 3 is in the "on" state. The decoupling capacitor 4 and the charge circuit 5 are therefore powered by the input voltage VIN in such a way as to improve the energy efficiency of the system SE.

[0035] If the input voltage VIN is already established when the switch circuit 3 turns on, the voltage VOUT present at the output terminal BS is less than the input voltage VIN present at the input terminal BE.

[0036] The positive rapid variation of the voltage applied $\Delta(VIN-VOUT)$ on the charge switch circuit 3 leads to a positive inrush current $CE+$ flowing from the input terminal BE to the output terminal BS in such a way as to charge the decoupling capacitor 4.

[0037] When the decoupling capacitor 4 is charged and when the input voltage VIN is set to zero more or less rapidly, the negative rapid variation of the voltage applied $\Delta(VIN-VOUT)$ on the charge switch circuit 3 leads to a negative inrush current $CE-$ flowing from the output terminal BS to the input terminal BE in such a way as to discharge the decoupling capacitor 4.

[0038] A control circuit is therefore provided, which is intended to limit these inrush currents and which will be described in greater detail hereinafter.

[0039] Reference is now made to FIG. 2 to illustrate very schematically an example of the charge switch circuit 3.

[0040] The charge switch circuit 3 comprises a charge switch should 6, a comparison stage 7, and a control circuit 8. The charge switch 6 comprises a MOS switching transistor TC of P type whose source is coupled to the input terminal BE, whose drain is coupled to the output terminal BS, and whose substrate is coupled to the larger of the input VIN and output VOUT voltages. The comparison stage 7 is configured to compare the input VIN and output VOUT voltages, and to deliver a selection signal SS as a function of the result of the comparison. The control circuit 8 is coupled to the gate G of the switching transistor TC and comprises a first adjustment stage ER1 and a second adjustment stage ER2.

[0041] The control circuit 8 is configured to activate the first or the second adjustment stage ER1 or ER2, as a function of the selection signal SS. Each adjustment stage ER1 or ER2 is configured to adjust the voltage of the gate of the switch 6 in such a way as to limit, respectively, the positive inrush current $CE+$ or the negative inrush current $CE-$.

[0042] By way of example, the control circuit 8 can furthermore comprise a control stage EC configured to selectively activate the first or the second adjustment stage ER1 or ER2, a first inverter stage EI1 whose output is coupled to the gate G of the switching transistor TC, and a